REMARKS

Claims 1-19 are pending. A minor amendment has been made to claim 11 in order to provide an antecedent basis for the term "data array". No new matter is being added.

Claims 1-10 and 16-19 are Allowed and claim 15 is indicated as allowable. Appreciation is expressed for the indication of allowance of these claims.

On page 3 of the Office Action, claims 11-14 are currently rejected under 35 USC § 102(e) as being anticipated by US 6,851,039 (hereinafter referred to as "Bickerstaff"). Applicants are traversing this rejection. Below, Applicants explain that Bickerstaff does not teach all of the elements of rejected claim 11.

Bickerstaff relates to, *inter alia*, an interleaved address generator (col. 7, line 9). As explained at col. 6, lines 43-45, a problem associated with interleaved address generators is that occasionally they generate addresses that are outside the valid range of a block size. Consequently, when an address is generated outside the range, a flag is generated that identifies if the address output is invalid (col. 6, lines 45-47). The address generator must then wait another clock cycle before the next sequential interleaved address is valid (col. 6, lines 47-49). Over a large block size, a large "overhead" in the turbo decoding process can be process (col. 6. lines 49-50). Col. 6, lines 50-65 and FIG. 5 relate to detail of how invalid addresses are generated during an interleaving process. A solution proposed by Bickerstaff (col. 6, lines 65-67) is to ensure that the address generator calculates <u>both</u> a current address and the next address at the same time. The first (current) address can thus be checked by the address interleaver and if the first address is invalid, the address interleaver can immediately substitute the next address, which was also generated at the same time (col. 7, lines 1-4).

Bickerstaff therefore proposes the address interleaver architecture of FIG. 6 thereof that generates both the current and next addresses at the same time (col. 7, lines 9-10). The architecture comprises parallel first look-up tables 10, 10' that generate a current inter-row <u>sequence number</u> and a next inter-row <u>sequence</u>

number (col. 7, lines 12-16), respectively. Parallel mod computation devices 12, 12' then generate a current <u>intra-row</u> permutation address and a next <u>intra-row</u> permutation address (col. 7, lines 16-20), respectively.

As described at col. 7, lines 23-24, a second look-up table 16' stores the intra-row <u>permutation sequences</u>. The second look-up table 16' outputs the current and next intra-row permutation <u>sequences</u> using the current and next <u>intra-row</u> permutation <u>addresses</u>. This is distinct from <u>interleaved</u> addresses. In this respect, <u>the second look-up table 16' does not receive interleaved addresses</u> (col. 7, lines 25-27).

Multipliers 18, 18' then receive current and next intra-row permutation <u>sequences</u> from the second look-up table 16' as well as an inter-row permutation pattern from a third look-up table (col. 7, lines 31-34). Clearly, the second look-up table 16' only outputs permutation <u>sequences</u> using <u>intra-row</u> permutation addresses and <u>interleaved addresses are not processed by the second look-up table16'</u>, which the Office Action alleges is equivalent to a buffer.

Indeed, as explained at col. 7, lines 35-36, it is the products generated by the multipliers 18, 18' that constitute the current and next interleaved addresses. <u>Consequently, no comparison is made by the second look-up table 16'</u>, because a comparison is made subsequently by the comparator 22 (col. 7, lines 40-47), which <u>necessarily</u> operates in combination with a comparator 60 as one of two addresses (generated in parallel as explained above) needs to be selected.

Referring to claim 11, claim 11 recites an interleaver for a turbo encoder and decoder comprising:

- at least one component adapted to provide valid and non-valid interleaved addresses; and
- a buffer arranged to store valid addresses and to output valid addresses at substantially constant rate; wherein

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- the buffer is adapted to compare received interleaved addresses with the size of a data array to determine a validity of a received address.

Hence, it is respectfully submitted that Bickerstaff fail to teach <u>a buffer adapted to compare received interleaved addresses with the size of a data array to determine a validity of a received address</u>, as recited in claim 1.

As stated above, the Office Action identifies the second look-up table 16' of Bickerstaff as the buffer that is recited in claim 1. However, as also stated above, the second look-up table 16' does not compare the received interleaved address with the size of a data array to determine the validity of a received address, because the second book-up table 16' does not receive interleaved addresses, only intra-row permutation sequences. Also, the second look-up table 16' does not perform a comparison function.

Claims 12-14 depend from claim 11. By virtue of this dependence, claims 12-14 are also novel.

The case is believed to be in condition for allowance and notice to such effect is respectfully requested. If there is any issue that may be resolved, the Examiner is respectfully requested to telephone the undersigned.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

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